

This listing of claims will replace all prior versions, and listings, of claims in the application:

LISTING OF THE CLAIMS:

Claim 1 (Currently amended) A metal oxide semiconductor (MOS) device comprising:
a semi-conducting substrate having source and drain regions;
a gate dielectric of less than 100 Å thickness on said semi-conducting substrate, said gate dielectric is selected from the group consisting of HfO₂, ZrO₃, Y₂O₃, silicates or nitrogen additions of HfO₂, ZrO₃, or Y₂O₃, and mixtures thereof; and
a Re-containing gate located directly on a surface of said gate dielectric, said Re-containing gate has an interface trapped charge density of about 3E 10 cm⁻² eV⁻¹ to about 4E 10 cm⁻² eV⁻¹ and a work function that ranges from about 4.6 eV to about 5.0 [[E]]eV and wherein said Re-containing gate is derived from a Re₂(CO)₁₀ CVD precursor.

Claim 2 (Previously Presented) A metal oxide semiconductor device according to claim 1, wherein said gate dielectric has a thickness of less than 50 Å.

Claim 3 (Cancelled)

Claim 4 (Cancelled)

Claim 5 (Cancelled)

Claim 6 (Cancelled)

Claim 7 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is p-type or n-type.

Claim 8 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 9 (Original) A metal oxide semiconductor device according to claim 1, wherein said semi-conducting substrate is formed of silicon.

Claim 10 (Previously presented) A field effect transistor (FET) comprising:
a semi-conducting substrate having at least one source and one drain region;
a gate dielectric layer of less than 100 Å thickness on said semi-conducting substrate,
said gate dielectric layer is selected from the group consisting of HfO₂, ZrO₃, Y₂O₃, silicates or nitrogen additions of HfO₂, ZrO₃, or Y₂O₃, and mixtures thereof; and
a Re-containing gate located directly on a surface of said gate dielectric layer, said Re-containing gate has an interface trapped charge density of about 3E 10 cm⁻² eV⁻¹ to about 4E 10 cm⁻² eV⁻¹ and a work function that ranges from about 4.6 eV to about 5.0 eV, and wherein said Re-containing gate is derived from a Re₂(CO)₁₀ CVD precursor.

Claim 11 (Previously Presented) A field effect transistor according to claim 10, wherein said gate dielectric layer has a thickness of less than 50 Å.

Claim 12 (Cancelled)

Claim 13 (Cancelled)

Claim 14 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is p-type or n-type.

Claim 15 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of a material selected from the group consisting of silicon, SiGe, SOI, Ge, GaAs, and organic semiconductors.

Claim 16 (Original) A field effect transistor according to claim 10, wherein said semi-conducting substrate is formed of silicon.

Claim 17 (Previously presented) A metal oxide semiconductor (MOS) device comprising:
a semi-conducting substrate having source and drain regions;
a Hf-based gate dielectric of less than 100 Å on said semi-conducting substrate; and
a Re-containing gate located directly on a surface of said Hf-based gate dielectric, said Re-containing gate has an interface trapped charge density of about 3E 10 cm⁻² eV⁻¹ to about 4E 10 cm⁻² eV⁻¹ and a work function ranging from about 4.6 eV to about 5.0 eV, and wherein said Re-containing gate is derived from a Re₂(CO)₁₀ CVD precursor.